Complementary Silicon High-Power Transistors

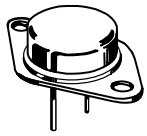
. . . PowerBase™ complementary transistors designed for high power audio, stepping motor and other linear applications. These devices can also be used in power switching circuits such as relay or solenoid drivers, dc–to–dc converters, inverters, or for inductive loads requiring higher safe operating area than the 2N3055.

- Current–Gain — Bandwidth–Product @ I_C = 1.0 Adc
  f_T = 0.8 MHz (Min) – NPN
  = 2.2 MHz (Min) – PNP
- Safe Operating Area — Rated to 60 V and 120 V, Respectively

NPN
2N3055A
MJ15015*
PNP
MJ15016*

*ON Semiconductor Preferred Device

15 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60, 120 VOLTS 115, 180 WATTS



CASE 1–07 TO–204AA (TO–3)

***MAXIMUM RATINGS**

Rating	Symbol	2N3055A	MJ15015 MJ15016	Unit
Collector–Emitter Voltage	V_{CEO}	60	120	Vdc
Collector–Base Voltage	V_{CBO}	100	200	Vdc
Collector–Emitter Voltage Base Reversed Biased	V_{CEV}	100	200	Vdc
Emitter–Base Voltage	V_{EBO}	7.0		Vdc
Collector Current — Continuous	I_C	15		Adc
Base Current	I_B	7.0		Adc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.65	180 1.03	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	0.98	°C/W

*Indicates JEDEC Registered Data. (2N3055A)

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

May, 2001 – Rev. 4
Publication Order Number:
2N3055A/D

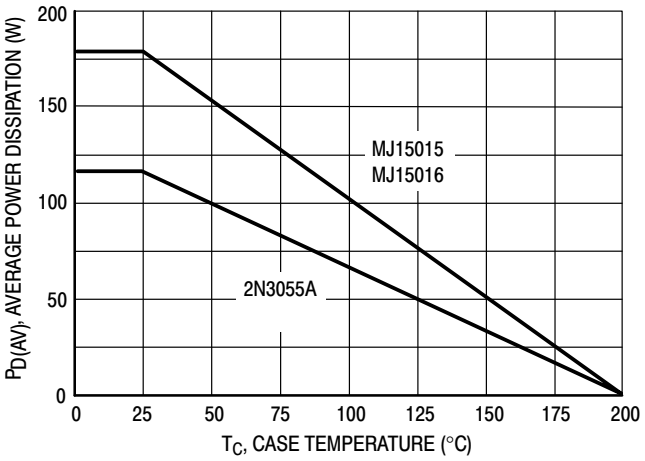


Figure 1. Power Derating

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS (1)					
*Collector–Emitter Sustaining Voltage (I_C = 200 mAdc, I_B = 0)	2N3055A MJ15015, MJ15016	$V_{CEO(sus)}$	60 120	— —	Vdc
Collector Cutoff Current		I_{CEO}			mAdc
(V_{CE} = 30 Vdc, $V_{BE(off)}$ = 0 Vdc)	2N3055A		—	0.7	
(V_{CE} = 60 Vdc, $V_{BE(off)}$ = 0 Vdc)	MJ15015, MJ15016		—	0.1	
*Collector Cutoff Current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)	2N3055A MJ15015, MJ15016	I_{CEV}	— —	5.0 1.0	mAdc
Collector Cutoff Current		I_{CEV}			mAdc
(V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	2N3055A MJ15015, MJ15016		— —	30 6.0	
Emitter Cutoff Current (V_{EB} = 7.0 Vdc, I_C = 0)	2N3055A MJ15015, MJ15016	I_{EBO}	— —	5.0 0.2	mAdc
***SECOND BREAKDOWN**					
Second Breakdown Collector Current with Base Forward Biased		$I_{S/b}$			Adc
(t = 0.5 s non–repetitive)	2N3055A		1.95	—	
(V_{CE} = 60 Vdc)	MJ15015, MJ15016		3.0	—	
***ON CHARACTERISTICS (1)**					
DC Current Gain		h_{FE}			—
(I_C = 4.0 Adc, V_{CE} = 2.0 Vdc)			10	70	
(I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)			20	70	
(I_C = 10 Adc, V_{CE} = 4.0 Vdc)			5.0	—	
Collector–Emitter Saturation Voltage		$V_{CE(sat)}$			Vdc
(I_C = 4.0 Adc, I_B = 400 mAdc)			—	1.1	
(I_C = 10 Adc, I_B = 3.3 Adc)			—	3.0	
(I_C = 15 Adc, I_B = 7.0 Adc)			—	5.0	
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)		$V_{BE(on)}$	0.7	1.8	Vdc
***DYNAMIC CHARACTERISTICS**					
Current–Gain — Bandwidth Product (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 MHz)	2N3055A, MJ15015 MJ15016	f_T	0.8 2.2	6.0 18	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)		C_{ob}	60	600	pF
***SWITCHING CHARACTERISTICS (2N3055A only)**					
RESISTIVE LOAD					
Delay Time	(V_{CC} = 30 Vdc, I_C = 4.0 Adc, I_{B1} = I_{B2} = 0.4 Adc, t_p = 25 μs Duty Cycle ≤ 2%)	t_d	—	0.5	μs
Rise Time		t_r	—	4.0	μs
Storage Time		t_s	—	3.0	μs
Fall Time		t_f	—	6.0	μs

(1) Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤ 2%.
*Indicates JEDEC Registered Data. (2N3055A)

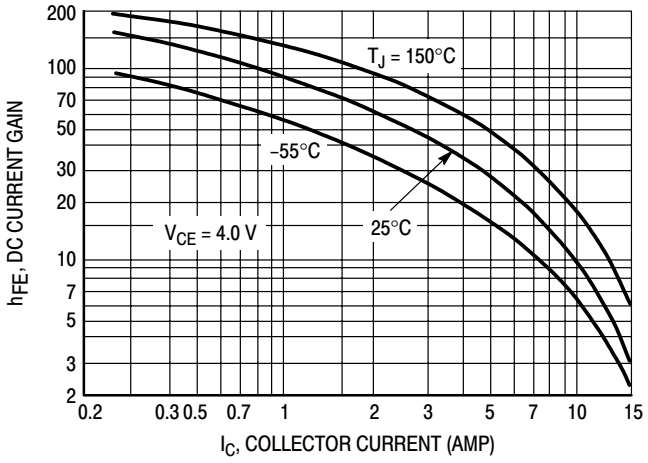


Figure 2. DC Current Gain

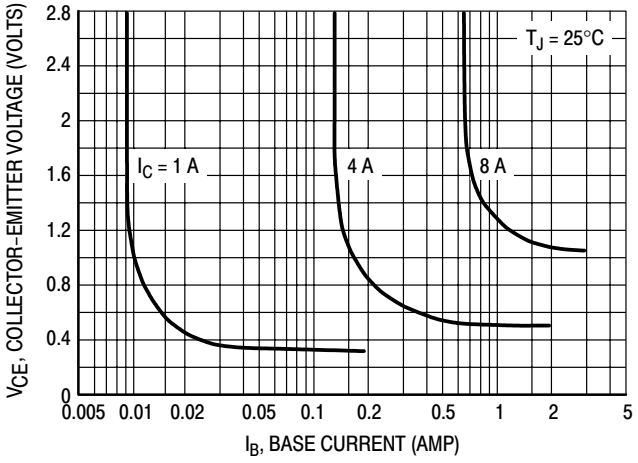


Figure 3. Collector Saturation Region

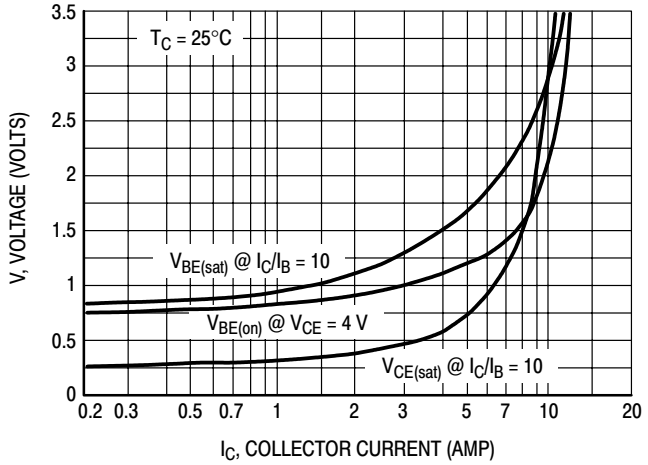


Figure 4. “On” Voltages

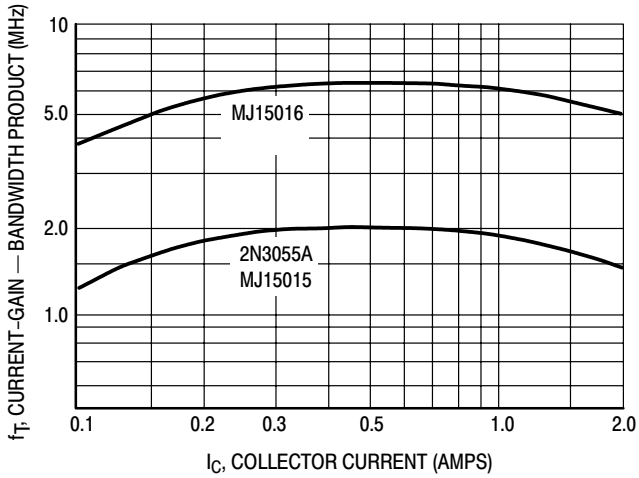


Figure 5. Current−Gain — Bandwidth Product

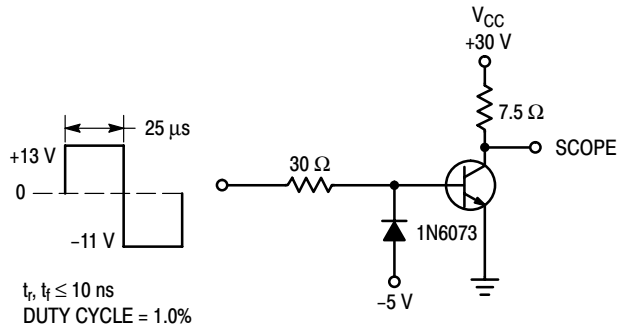


Figure 6. Switching Times Test Circuit (Circuit shown is for NPN)

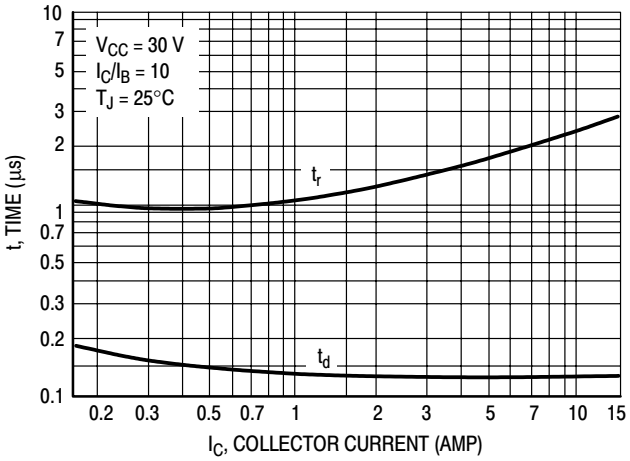


Figure 7. Turn−On Time

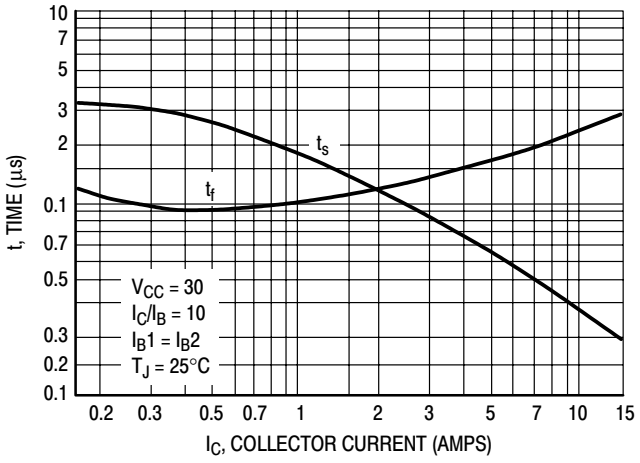


Figure 8. Turn–Off Times

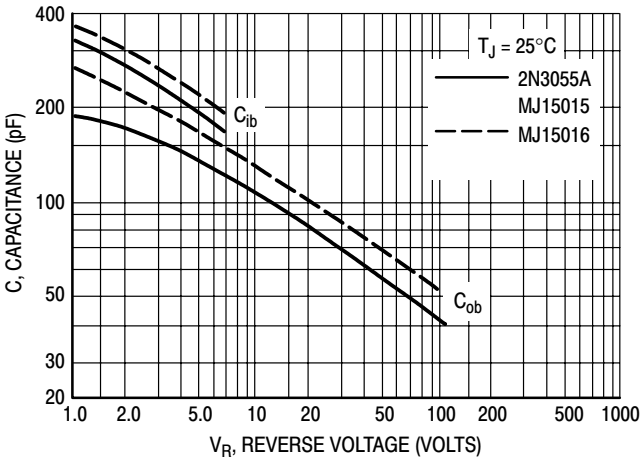


Figure 9. Capacitances

COLLECTOR CUT–OFF REGION

NPN

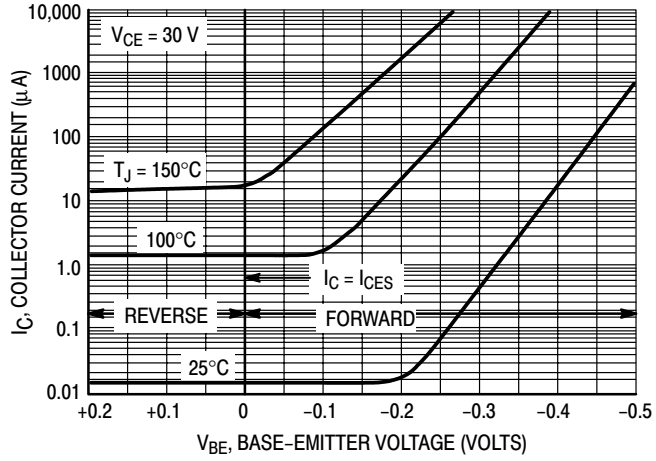


Figure 10. 2N3055A, MJ15015

PNP

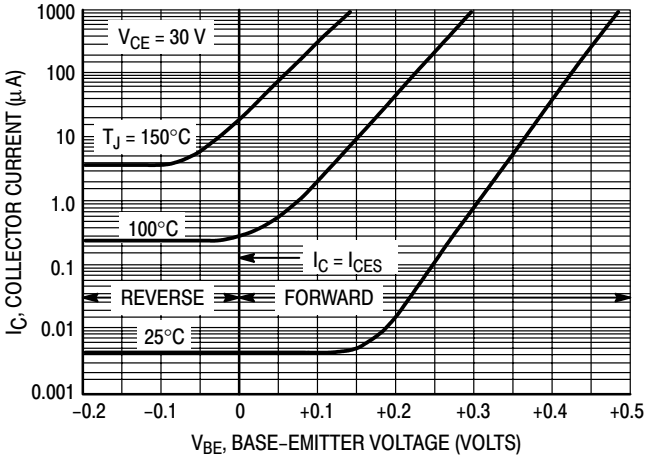


Figure 11. MJ15016

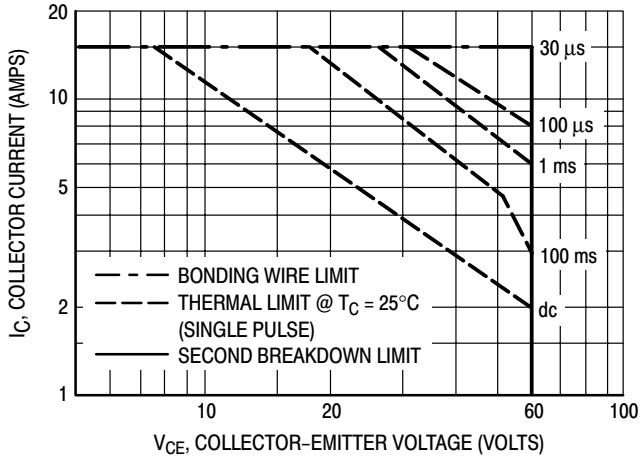


Figure 12. Forward Bias Safe Operating Area 2N3055A

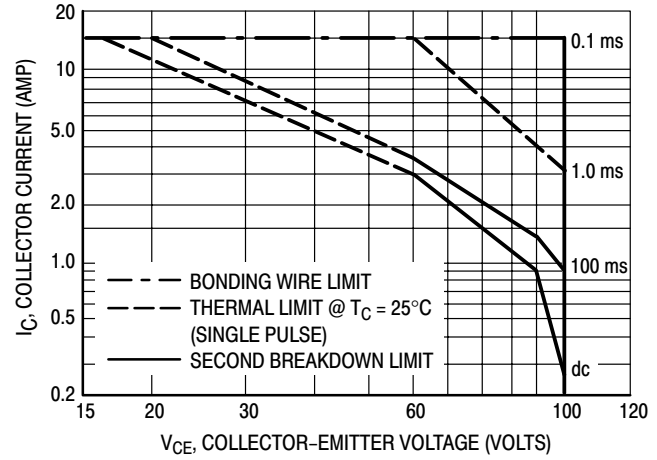


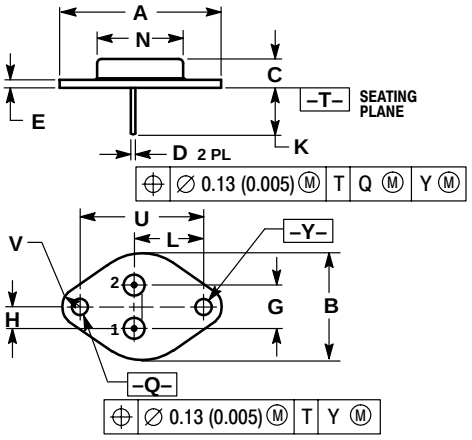
Figure 13. Forward Bias Safe Operating Area MJ15015, MJ15016

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe Operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 12 and 13 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

PACKAGE DIMENSIONS

CASE 1–07
TO–204AA (TO–3)
ISSUE Z



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO–204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

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